ISSN 2229-5518

# Reduced SCEs in Fully Depleted Dual-Material Double-Gate (DMDG) SON MOSFET: Analytical Modeling and Simulation

Saheli Sarkhel, Sounak Naha, Subir Kumar Sarkar

**Abstract**— In this paper, a two dimensional analytical model of a fully depleted nano-scale dual material double gate (DMDG) SON MOSFET has been developed and performance comparison is made with single material double gate SON MOSFET. An expression for the electric field has also been developed. It is found that the introduction of the DMDG structure in a fully depleted SON MOSFET leads to reduction of short channel effects due to a step-function in the surface potential profile thereby improving device performance and enhances devices scalability some steps further with the extreme exploitation of the idea, threshold control by means of multiple material gate electrode.

**Index Terms**— Fully depleted, Double Gate (DG), Dual Material gate (DMG), Analytical Modeling, Short channel effects (SCEs), SON MOSFET, Two Dimensional Modeling.

---

## 1 Introduction

WITH the emergence of mobile computing and communication, low power device design and implementation have got a significant role to play in VLSI circuit design. Continuous device performance improvement is possible only through a combination of device scaling, new device structures and material property improvement to its fundamental limits [1], [2]. As downscaling continues, the issue of power dissipation is becoming one of the two most important issues (other being the speed). The ever decreasing device dimensions have reached a state where the performance of the bulk *Si MOSFETs* is limited by the fundamental physical limits such as reduction in carrier mobility due to impurities, increasing gate tunneling effect as the gate oxide thickness decreases and increasing *p-n* junction leakage current as the junctions become more and more shallow. These requirements have led to development of alternative technologies. *SOI* technology is one such alternative which can offer a performance as expected from next generation *Si* technology. Short-channel-effects (SCEs), transistor scalability, speed of operation and circuit performance are improved by using SOI technology, especially ultrathin, fully depleted (FD) MOSFETs [3]. However to overcome the SCEs to a larger extent different modifications in the SOI technology is required [4]. Silicon-on-Nothing (SON), an innovative SOI structure suggested and developed very recently, is capable of quasitotal suppression of SCEs and excellent electrical performances [5]. Among the advantages of fully-depleted (FD) SON architecture compared to FDSOI, the most significant one is the reduced electrostatic coupling of channel with source/drain and substrate through the buried layer (BL) [6]. Thick buried layer can be a drawback of SOI MOSFETs due to large positive charge accumulated in the thick BL, while no charge will be accumulated in the air-gap in the case of a SON MOSFET.

Double Gate (DG) MOSFETs using lightly doped ultra thin layers seem to be a very promising option for ultimate scaling of CMOS technology [7]. In particular, asymmetrical DG SOI MOSFETs (front gate p+ poly and back gate n+ poly) are becoming popular since this type of structure provides a desirable threshold voltage (not too high or too low) unlike the symmetrical DG SOI MOSFETs.

As the channel length shrinks, the control of gate voltage on the threshold voltage decreases due to increased charge sharing from source and drain. Therefore, the threshold voltage reduction with decreasing channel lengths and drain induced barrier lowering (DIBL) are important issues that need to be addressed while providing immunity against short-channel effects (SCEs) [8]. To enhance the immunity against short channel effects, a new structure called dual material gate (DMG) MOSFET was proposed [10]. The structure, which uses two metals in the gate M1 and M2 with different work functions, provides simultaneous increase in transconductance and suppressed SCEs.

In the DMG structure, the peak electric field at the drain end is reduced which ensures that the average electric field under the gate is increased [8]. The step in the potential profile ensures screening of the channel region under the gate material on the source side (M1) from variations in the drain potential. To incorporate the advantages of SON, DG and DMG structures, we, in this paper, propose a new structure for dual material double gate (DMDG) nanoscale SON MOSFETs. The rest of the paper has been arranged as follows: In section 2, a two dimensional analytical model for surface potential using Poisson's equation has been presented. The


- *Saheli Sarkhel is currently pursuing M. Tech in VLSI design and Microelectronics Technology from Jadavpur University, India, E-mail: saheli.sarkhel@gmail.com*
- *Sounak Naha is currently pursuing M. E. in Electronics and Communication Engineering from Jadavpur University, India, E-mail: sounaknaha@gmail.com*
- *Subir Kumar Sarkar is currently a Professor and the Head of the department of Electronics & TelecommunicationEngineering in Jadavpur University. E-mail: su_sircir@yahoo.co.in*

results and explanations are given in section 3. Section 4 concludes the paper.

## 2 Analytical Modeling

A schematic cross-sectional view of a DMDG FD SON MOSFET is shown in Fig.1. The front gate consists of dual materials M1 and M2 of lengths L1 and L2 respectively while the back gate is material M2. We have used $p^+$ poly as M1 and $n^+$ poly as M2. Assuming the impurity density in the channel region to be uniform, and neglecting the effect of the fixed oxide charges on the electrostatics of the channel, the potential distribution in the silicon thin film before the onset of strong inversion can be written as [8]:

$$\frac{d^2\phi(x,y)}{dx^2}+\frac{d^2\phi(x,y)}{dy^2}=\frac{qN_A}{\varepsilon_{Si}} \quad (1)$$

Where Φ (x, y) is the two dimensional potential profile in the silicon channel, $N_A$ is the uniform film doping concentration independent of the gate length, $\varepsilon_{Si}$ is the dielectric constant of silicon, $t_{Si}$ is the film thickness and L is the device channel length. Considering a second order potential approximation, Φ (x, y) can be approximated by a simple parabolic function as proposed by [8].

$$\Phi(x,y)=\Phi_s(x)+c_1(x)y+c_2(x)y^2 \quad (2)$$

Where $\Phi_S$ (x) is the surface potential, $c_1$ (x) and $c_2$ (x) are x dependent arbitrary coefficients.

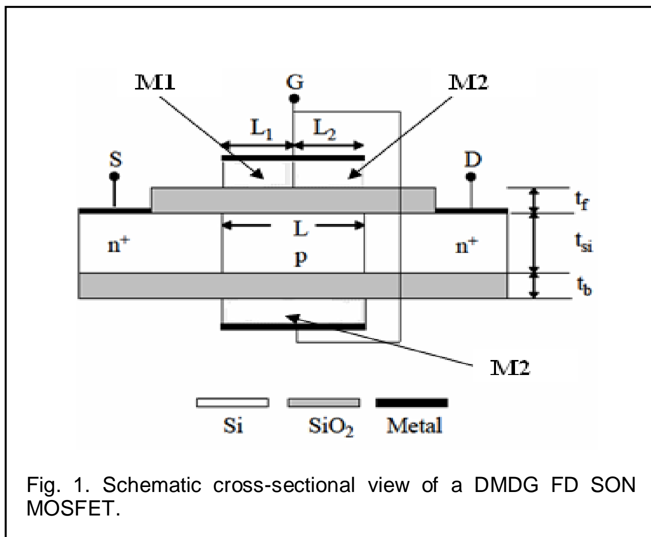


Fig. 1. Schematic cross-sectional view of a DMDG FD SON MOSFET.

Since we have two regions in the front gate of the DMDG structure, the surface potential under M1 and M2 can be written based on (2) as

$$\Phi(x,y)=\Phi_{S1}(x)+c_{11}(x)y+c_{12}(x)y^2 \quad (3)$$

$$\Phi(x,y)=\Phi_{S2}(x)+c_{21}(x)y+c_{22}(x)y^2 \quad (4)$$

Where $\phi_{M1}$ and $\phi_{M2}$ are the surface potentials under p+ poly (M1) and n+ poly (M2) respectively, $\phi_{Si}$ is the silicon work function and $c_{11}$, $c_{12}$, $c_{21}$ and $c_{22}$ are arbitrary coefficients. Depending on the continuity of electrostatic potential, the four boundary conditions used here are as follows:

1. For dual material gate at the front surface, the electric flux is continuous at the at the front gate oxide. So,

$$\left.\frac{d\phi_1(x,y)}{dy}\right|_{y=0}=\frac{\varepsilon_{oxf}}{\varepsilon_{Si}}\frac{\phi_{s1}(x)-V'_{G1}}{t_f}, \text{under}M1 \quad (5)$$

$$\left.\frac{d\phi_2(x,y)}{dy}\right|_{y=0}=\frac{\varepsilon_{oxf}}{\varepsilon_{Si}}\frac{\phi_{s2}(x)-V'_{G2}}{t_f}, \text{under}M2 \quad (6)$$

, where $\varepsilon_{oxf}$ is the dielectric constant of the oxide ($SiO_2$) at the front gate and $t_f$ is the oxide thickness, and

$V'_{G1}=V_{GS}-V_{FBfp}, V'_{G2}=V_{GS}-V_{FBfn}$,

, where $V_{GS}$ is the gate-to-source bias voltage and $V_{FBfp}$ and $V_{FBfn}$ are the front channel flat-band voltages of the $p^+$ poly and $n^+$ poly respectively and

$V_{FBfp}=\phi_{M1}-\phi_{Si}, V_{FBfn}=\phi_{M2}-\phi_{Si}$

2. The electric flux at the back gate oxide and back channel interface is continuous for both the materials at the front gate

$$\left.\frac{d\phi_1(x,y)}{dy}\right|_{y=t_{Si}}=\frac{\varepsilon_{oxb}}{\varepsilon_{Si}}\frac{V'_{GSb}-\phi_B(x)}{t_b}, \text{under}M1 \quad (7)$$

$$\left.\frac{d\phi_2(x,y)}{dy}\right|_{y=t_{Si}}=\frac{\varepsilon_{oxb}}{\varepsilon_{Si}}\frac{V'_{GSb}-\phi_B(x)}{t_b}, \text{under}M2 \quad (8)$$

, where $\varepsilon_{oxb}$ is the dielectric constant of the oxide (here for DMDG SON, air is taken as the back gate oxide at the front gate and $t_b$ is the back oxide thickness, $\phi_B$ (x) is the potential function along the back gate oxide -silicon interface, and $V'_{GSb}=V_{GS}-V_{FBbn}$, where $V_{FBbn}$ is the back gate flat-band voltage and is same as that of $V_{FBfn}$.

3. At the front gate, the surface potential at the interface of two dissimilar gate materials is continuous.

$$\Phi_1(L_1, 0)=\Phi_2(L_1, 0) \quad (9)$$

4. At the front gate, the electric flux is continuous at the interface of two different gate materials.

$$\left.\frac{d\phi_1(x,y)}{dx}\right|_{x=L_1}=\left.\frac{d\phi_2(x,y)}{dx}\right|_{x=L_1} \quad (10)$$

5. The potential at the source end is

$$\Phi_1(0, 0)=\Phi_{S1}(0)=V_{bi} \quad (11)$$

, where $V_{bi}$ is the built in potential across the body-source junction.

6. The potential at the drain end is

$$\Phi_2(L_1+L_2, 0)=\Phi_{S2}(L_1+L_2)=V_{bi}+V_{DS} \quad (12)$$

, where $V_{DS}$ is the applied drain to source voltage.

The coefficients $c_{11}$, $c_{12}$, $c_{21}$ and $c_{22}$ are all functions of x and their values are calculated using boundary conditions. Substituting these values in equation (3) and (4) and then in (1), two second order differential equations are obtained as:

ISSN 2229-5518

$$\frac{d^2\phi_{s1}(x)}{dx^2}+\alpha\phi_{s1}(x)=\beta_1,\text{underM1} \tag{13}$$

$$\frac{d^2\phi_{s2}(x)}{dx^2}+\alpha\phi_{s2}(x)=\beta_2,\text{underM2} \tag{14}$$

, where

$$\alpha=\frac{2[1+C_f/C_{Si}+C_f/C_b]}{t_{Si}{}^2(1+2C_{Si}/C_b)}$$

$$\beta_1=\frac{qN_A}{\varepsilon_{Si}}-\frac{2V'_{G1}\left[\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right]}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}-\frac{2V'_{GSb}}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}$$

$$\beta_2=\frac{qN_A}{\varepsilon_{Si}}-\frac{2V'_{G2}\left[\frac{C_f}{C_b}+\frac{C_f}{C_{Si}}\right]}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}-\frac{2V'_{GSb}}{t_{Si}^2\left(1+\frac{2C_{Si}}{C_b}\right)}$$

Here $C_{Si}$ is the channel depletion layer capacitance, $C_f$ is the front interface capacitance and $C_b$ is the buried layer (back gate in this case) oxide capacitance. Solving the second order differential equation, we obtain the expressions for surface potential under M1 and M2 of the front gate are given by:

$$\phi_{S1}(x)=A\exp(\eta x)+B\exp(-\eta x)-\frac{\beta_1}{\alpha}$$

$$,for\ 0\le x\le L_1,under M_1 \tag{15}$$

$$\phi_{S2}(x)=C\exp(\eta(x-L_1))+D\exp(-\eta(x-L_1))-\frac{\beta_2}{\alpha}$$

$$,for\ L_1\le x\le L,under M_2 \tag{16}$$

, where

$$A=\left[(V_{bi}+V_{DS}+\sigma_2)-(V_{bi}+\sigma_1)e^{-\eta L}\right.$$
$$\left.+(\sigma_1-\sigma_2)\cosh(\eta L_2)\right]\left\{\frac{e^{-\eta L}}{1-e^{-2\eta L}}\right\}$$

$$B=\frac{(V_{bi}+\sigma_1)-(V_{bi}+V_{DS}+\sigma_2)e^{-\eta L}-(\sigma_1-\sigma_2)\cosh(\eta L_2)e^{-\eta L}}{1-e^{-2\eta L}}$$

$$C=A\exp(\eta L_1)-\frac{\sigma_1-\sigma_2}{2}$$

$$D=B\exp(-\eta L_1)-\frac{\sigma_1-\sigma_2}{2}$$

$$\sigma_1=\frac{\beta_1}{\alpha},\sigma_2=\frac{\beta_2}{\alpha},\eta=\sqrt{\alpha}$$

The electric field variation along the channel length can also be obtained by differentiating the expression of surface potential and can be expressed as

$$E_1(x)=A\eta\exp(\eta x)-B\eta\exp(-\eta x),\text{underM1} \tag{17}$$

$$E_2(x)=C\eta\exp(\eta(x-L_1))-D\eta\exp(-\eta(x-L_1)),\text{underM2} \tag{18}$$

## 3 Results and Discussions

We have considered a dual material double gate SON structure for analytical simulation. The channel length is taken as 100 nm for the calculations. The different materials that are considered for the gate as M1 and M2 are $p^+$ poly and $n^+$ poly respectively. Different parameters that we have used in the calculation are given in table 1.

TABLE 1
DIMENTION TABLE

| Parameter | Value |
|---|---|
| $V_{gs}$ | 0.15 V |
| $N_d$ | $5\times10^{23}$ $m^{-3}$ |
| $N_a$ | $10^{21}$ $m^{-3}$ |
| $N_i$ | $1.5\times10^{15}$ $m^{-3}$ |
| $t_f$ | 2nm |
| $t_b$ | 2 nm |
| $t_{Si}$ | 12 nm |
| $\phi_{M1}$ ($p^+$ poly) | 5.25 eV |
| $\phi_{M2}$ ($n^+$ poly) | 4.17 eV |

In Fig.2 the calculated values of surface potential are plotted with respect to the position along the channel of the FD DMDG SON for channel length L=100 nm at different drain to source voltages. It is observed that the surface potential at the center exhibits a step function in the surface. Due to this step function, the area under M1 of front gate of the DMDG structure is screened from the drain potential variations. Thus, the step function suppresses the effect of the electric field induced by the drain-source potential in the region under M1 and hence, there is no significant change in the surface potential under M1 as we increase the drain bias.

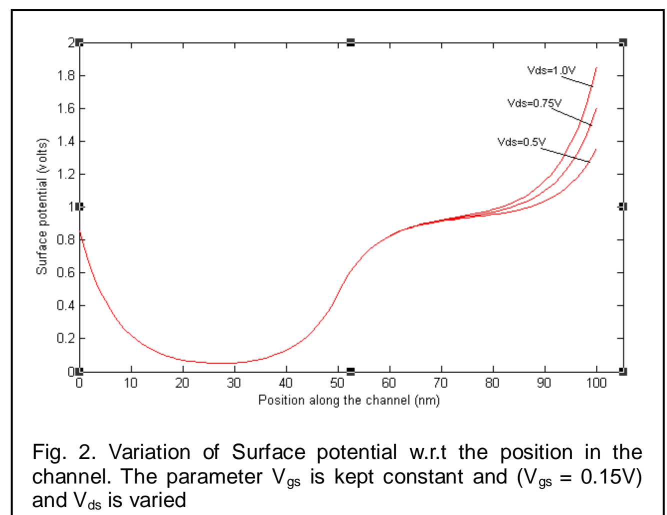


Fig. 2. Variation of Surface potential w.r.t the position in the channel. The parameter $V_{gs}$ is kept constant and ($V_{gs}$ = 0.15V) and $V_{ds}$ is varied

This means that drain potential has a very little effect on

the drain current after saturation [10] which in turn considerably reduces the drain conductance and DIBL effect for the DMDG SON MOSFET.

Fig. 3 compares the surface potential profile with respect to channel position for different combinations of gate lengths $L_1$ and $L_2$, keeping the total gate length of the DMDG SON MOSFET to be constant and the surface potential profile with respect to channel position of a DG SON MOSFET. It is seen from the figure that in the second case there is no change in the surface potential but in the first case, the position of minimum surface potential, lying under $M_1$ is shifting toward the source as the length of gate $M_1$ is reduced. This causes the peak electric field in the channel to shift more toward the source end and thus there is a more uniform electric field profile in the channel. Moreover, it is observed that the channel potential minima for the three cases are not the same. This happens because as $L_1$ increases, the portion of the channel controlled by the gate metal with larger work-function is increased.

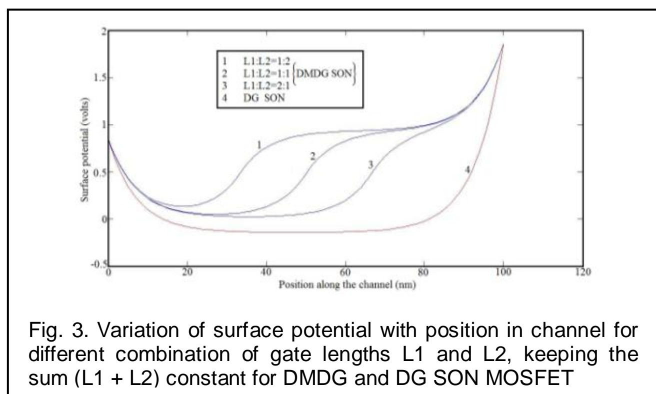


Fig. 3. Variation of surface potential with position in channel for different combination of gate lengths L1 and L2, keeping the sum (L1 + L2) constant for DMDG and DG SON MOSFET

In Fig.4 we have plotted the electric field along the channel length and the nature of electric field variation under M2 is shown. Due to the presence of discontinuity in the surface potential of the DMDG SON MOSFET, the peak electric field near the drain side is substantially reduced for the DMDG devices when compared with that of their DG counterpart. This causes the DMDG devices to achieve simultaneous suppression of the short-channel effects and hot-carrier effects.

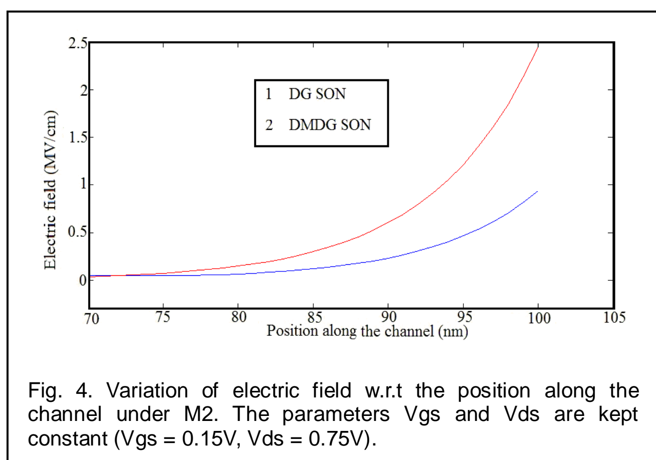


Fig. 4. Variation of electric field w.r.t the position along the channel under M2. The parameters Vgs and Vds are kept constant (Vgs = 0.15V, Vds = 0.75V).

It is quite evident from the figure that the peak electric field at the drain end is reduced considerably due to the presence of a gate material with lower work function than the gate material at the source end.

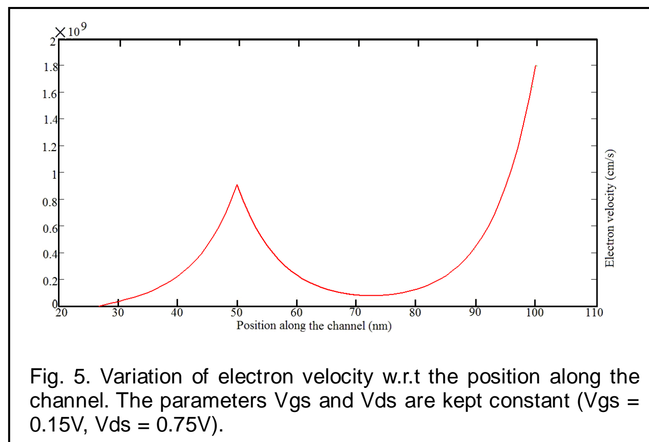


Fig. 5. Variation of electron velocity w.r.t the position along the channel. The parameters Vgs and Vds are kept constant (Vgs = 0.15V, Vds = 0.75V).

In Fig.5, the variation of electron velocity along the channel length has been shown. It is evident from the figure that the nature of the electron velocity distribution resembles that of the electric field distribution in the sub-threshold regime. This type of electron velocity distribution at the source side has an important effect on the overall carrier transport efficiency of the DMDG device [11].

## 4 Conclusion

Here, we have developed a 2-D analytical model for surface potential and examined the effectiveness of the DMG structure in the front gate of fully depleted SON MOSFETs to suppress Short Channel Effects (SCEs). The results obtained from the analytical model unambiguously establish that the introduction of the DMG structure in the front gate of the fully depleted SON MOSFET leads to subdued SCEs due to a step-function in the channel potential profile at the interface of two materials. The shift in the surface channel potential minima position is negligible with increasing drain biases. Moreover, the peak electric field at the drain end is reduced as compared to that using a single material in the front gate, thus minimizing the hot carrier effect. Thus, the introduction of the DMG structure in the front gate of the fully depleted DG SON MOSFETs improves the short-channel behavior of the SON MOSFETs over their single-material front gate in DG SON and the bulk counterparts.

## Acknowledgment

The authors thankfully acknowledg the financial support obtained from DRDO vide order no. EIRP/ER/1103935M/01/1344 dated 28/06/2011.

## References

[1] S.Deb, N.B.Singh, D.Das, A.K.De, S.K.Sarkar, "Analytical model of Threshold Voltage and Sub-threshold Slope of SOI and SON MOSFETs: A comparative study", *Journal of Electron Devices*, Vol. 8, pp. 300-309, 2010.

[2] The International Technology Roadmap for Semiconductor, Emerging Research Devices, 2009.

[3] M.Current, S.Bebell, I.Malik, L.Feng, F.Henley, "What is the future of sub-100nm CMOS: Ultrashallow junctions or ultrathin SOI ?", Solid State Technology, 2000; 43,.

[4] J.Pretet,S.Monfray,S.Cristoloveanu,T.Skotnicki, "Silicon-on-Nothing MOSFETs: Performance, Short-Channel Effects, and Backgate Coupling", *IEEE Transactions on Electron Devices*, 2004; 51(2), 240-246.

[5] M.Jurczak,T.Skotnicki,M.Paoli,B.Tormen,J.Martins,J.Regolini, D.Dutartre,P.Roibot,D.Lenoble,R.Pantel,S.Monfray, "Silicon-on-Nothing (SON)-an Innovative Process for Advanced CMOS", *IEEE Transactions on Electron Devices*, 2000; 47(11), 2179-2187.

[6] T.Sato,H.Nii,M.Hatano,K.Takenaka,H.Hayashi,K.Ishigo,T.Hirano, K.Ida,Y.Tsunashima, "Fabrication of SON (Silicon on Nothing)-MOSFET and Its ULSI Applications", *IEIC Technical Report*,2002;102(178); (SDM2002 66-106);99-104.

[7] D.J.Frank, R.H.Dennard, E.Nowak, D.M.Solomon, Y.Taur, and H.Wong, "Devicescaling limits of Si MOSFETs and their application dependencies" , *Proc. IEEE*, vol.89,pp.259-288, 2001.

[8] G. Venkateshwar Reddy and M. Jagadesh Kumar , " A New Dual-Material Double-Gate (DMDG) Nanoscale SOI MOSFET- Two Dimensional Analytical Modeling and Simulation, " *IEEE Trans. on Nanotechnology*, Vol. 4, pp.260-268, /March 2005.

[9] A. Chaudhry and M. J. Kumar, "Controlling Short-channel Effects in Deep Submicron SOI MOSFETs for Improved Reliability: A Review", *IEEE Trans. on Device and Materials Reliability,* Vol.4, pp.99-109, March 2004.

[10] M. J. Kumar and A. Chaudhry, "Two-Dimensional Analytical Modeling of Fully Depleted Dual-Material Gate (DMG) SOI MOSFET and Evidence for Diminished Short-Channel Effects", *IEEE Tran. on Electron Devices,* Vol.15, pp.569-574, April 2004.

[11] K. Goel, M. Saxena, M. Gupta, and R. S. Gupta, "Modeling and simulation of a nanoscale three-region tri-material gate stack (TRIMGAS) MOSFET for improved carrier transport efficiency and reduced hotelectron effects," *IEEE Trans. Electron Devices*, vol. 53, no. 7, pp. 1623–1633, Jul. 2006.